IN THE CLAIMS:

Please amend the claims as follows:

1.   (Currently Amended) An improved A digital-data receiver synchronization apparatus comprising:

    a plurality of memory devices for receiving multiple timing signals; and

    a feedback means circuit interconnecting said plurality of memory devices and cross-coupling signals produced by said plurality of memory devices.

2.   (Currently Amended) The improved digital-data receiver synchronization apparatus of claim 1, further comprising:

    a common frequency reference source in communication with said plurality of memory devices, said common frequency reference source for driving said plurality of memory devices.

3.   (Currently Amended) The improved digital-data receiver synchronization apparatus of claim 2 1, wherein said multiple timing signals include at least one signal selected from the group consisting of an RF carrier signal, a data bit-rate signal, a data chip-rate signal, a data frame-rate signal, and a data burst-rate signal or and a packet-rate signal.

4.   (Currently Amended) The improved digital-data receiver synchronization apparatus of claim 2, wherein said multiple timing signals are integrally or fractionally related in frequency, phase or both frequency and phase.

5.   (Currently Amended) The ~~improved~~ digital-data receiver synchronization apparatus of claim 2, wherein said multiple timing signals are rationally ~~multiply~~ related in frequency and/or phase.

6.   (Currently Amended) The ~~improved~~ digital-data receiver synchronization apparatus of claim 2 <u>3</u>, wherein said multiple timing signals satisfy <u>a</u> ~~the~~ relationship

$$f_1 = M{\cdot}f_2 = M{\cdot}N{\cdot}f_3$$

wherein f_1 is said RF <u>carrier</u> signal; f_2 is said data bit-rate signal; f_3 is said data frame-rate signal; and M and N are positive rational numbers.

7.   (Currently Amended) The ~~improved~~ digital-data receiver synchronization apparatus of claim 2, wherein said common frequency reference <u>source includes</u> ~~is~~ an oscillator controlled by a crystal, SAW device, ceramic resonator, mechanical resonator, dielectric resonator, or external source.

8.   (Currently Amended) The ~~improved~~ digital-data receiver synchronization apparatus of claim 2, wherein said common frequency reference <u>source</u> uses edge-triggered synchronous logic.

9.   (Currently Amended) The ~~improved~~ digital-data receiver synchronization apparatus of claim 2 <u>1</u>, wherein ~~said~~ signals cross-coupled by said feedback ~~means~~ <u>circuit</u>

include at least one ~~signal~~ <u>member</u> selected from the group consisting of error signals,~~output~~

~~signals, and both error~~ and output signals.

10.   (Currently Amended) The ~~improved~~ digital-data receiver synchronization

apparatus of claim 1, wherein ~~said~~ signals cross-coupled by said feedback ~~means are~~ <u>circuit</u>

<u>include</u> analog signals.

11.   (Currently Amended) The ~~improved~~ digital-data receiver synchronization of claim

1, wherein ~~said~~ signals cross-coupled by said feedback ~~means are~~ <u>circuit include</u> digital signals.

12.   (Currently Amended) The ~~improved~~ digital-data receiver synchronization

apparatus of claim 1, wherein said <u>plurality of</u> memory devices ~~are~~ <u>include</u> phase-locked loops.

13-26. (Canceled)

27.   (Currently Amended) ~~The~~ <u>A</u> method of providing improved digital-data receiver

synchronization comprising ~~the steps of~~:

providing a plurality of memory devices for receiving multiple timing signals, at least one

of said plurality of memory devices comprising a composite phase-frequency detector, each of

said plurality of memory devices providing an output comparison signal; and~~,~~

interconnecting said <u>plurality of</u> memory devices with a feedback ~~means~~ <u>circuit</u> ~~for~~ <u>that</u>

<u>cross-couples</u> ~~cross-coupling~~ said output comparison signals produced by <u>each of</u> said <u>plurality</u>

<u>of</u> memory devices.

28.   (Currently Amended) The method according to claim 27, further comprising ~~the step of~~:

connecting a common frequency reference source <u>to</u> ~~with~~ said plurality of memory devices<u>, said common frequency reference source</u> ~~for~~ driving said plurality of memory devices.

29.   (Canceled)